

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of Docket No: Q77597
Yasushi KINOSHITA Allowed: November 19, 2007
Appln. No.: 10/669,655 Group Art Unit: 2811
Confirmation No.: 5578 Examiner: Samuel A. GEBREMARIAM
Filed: September 25, 2003 Issued: April 8, 2008
U.S. Patent No.: 7,355,265

For: SEMICONDUCTOR INTEGRATED CIRCUIT

SUBMISSION OF ART

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

For the possible benefit of anyone subsequently evaluating the scope and/or validity of the above-identified patent, it is requested that the documents that are listed below be placed in the U.S. Patent and Trademark Office's file wrapper of the above-identified U.S. patent:

1. Japanese Patent Application Laid-Open No. 10-41468, published February 13, 1998.
2. Japanese Patent Application Laid-Open No. 2000-58759, published February 25, 2000.

The above-listed documents were recently cited in a corresponding Japanese Office Action, dated February 19, 2008, a copy of which is enclosed.

SUBMISSION OF ART
U.S. Application No.: 10/669,655

Attorney Docket No.: Q77597

The undersigned has not reviewed the teachings of the above-listed documents in detail and thus makes no representations concerning the relevancy or materiality of the above-listed documents.

This is not an Information Disclosure Statement and no response from the U.S. Patent and Trademark Office is believed to be necessary, nor are any fees believed to be due.

Respectfully submitted,

/Howard L. Bernstein/

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Date: April 15, 2008